

## ABSTRACT OF THE DISCLOSURE

A processing apparatus includes a memory capable of storing data, a butterfly arithmetic unit for performing butterfly computation processes, and a bit-reversed order shuffle processing unit for writing results obtained by butterfly computation processes performed by the butterfly arithmetic unit at addresses in the memory after bit-reversed order shuffle instead of writing the results at addresses in the memory in processing order. The data written by the bit-reversed order shuffle processing unit are discrete fast Fourier transform results.